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| EXAMINER | |
|---|---|
| THANGAVELU, KANDASAMY | |

| ART UNIT | PAPER NUMBER |
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| 2123 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/273,560 | HASEGAWA, TAKUMI | |
| | Examiner | Art Unit | |
| | KANDASAMY THANGAVELU | 2123 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Introduction*

1. This communication is in response to the Applicants' Amendment dated February 15, 2008. Claims 1-4 of the application were amended. Claims 5-6 were added. Claims 1-6 of the application are pending. This office action is made non-final.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the first paragraph of 35 U.S.C. §112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 5-6 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

3.1 Claim 5 states, "The delay analysis system as set forth in claim l, wherein the delay analyzing module determines automatically, based on the logical operation information of the logical circuit, that there is no change in a signal state of an output terminal of the logical circuit,

and when no change in the signal state is determined, the delay analyzing module determines that no further delay analysis needs to be performed". The Examiner checked carefully the entire specification and found that there is no support for determining automatically, based on the logical operation information of the logical circuit, that there is no change in a signal state of an output terminal of the logical circuit, and when no change in the signal state is determined, the delay analyzing module determining that no further delay analysis needs to be performed in the application. This is new material introduced in the current amendment and is not allowed.

3.2 Claim 6 states, "The delay analysis system as set forth in claim 5, wherein the logical circuit is an AND gate, and when the logical operation information of the AND gate in the delay analysis library indicates that the state of the output terminal of the AND gate changes LOW-HIGH- LOW within a period of two clock signals, and at a time at which the second clock signal among the two clock signals is input, the state is LOW which is regarded to be the same state as the first signal state, the delay analysis library does not recognize a rise (LOW-HIGH) at the output terminal of the AND gate corresponding to a clock signal, the delay time information of the AND gate is labeled as NONE indicating no change in the signal state at the output terminal of the AND gate, and the delay analyzing module, based on the delay time information labeled as NONE, automatically determines that no further delay analysis needs to be performed in this case". The Examiner checked carefully the entire specification and found that there is no support for the delay analysis library not recognizing a rise (LOW-HIGH) at the output terminal of the AND gate corresponding to a clock signal, the delay time information of the AND gate being labeled as NONE indicating no change in the signal state at the output terminal of the

AND gate, and the delay analyzing module, based on the delay time information labeled as NONE, automatically determining that no further delay analysis needs to be performed in this case in the application. This is new material introduced in the current amendment and is not allowed.

***Claim Rejections - 35 USC § 101***

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 1-3 and 5-6 are rejected under 35 U.S.C. 101 because the claimed inventions are directed to non-statutory subject matter.

5.1 Claim 1 states, "A delay analysis system for making a delay analysis of a logic circuit, said system comprising:

a delay analysis library comprising connection information and delay time information for a plurality of circuits; and

a delay analyzing module which analyzes delays of the plurality of the circuits based on information in the delay analysis library, …;

wherein the delay analyzing module analyzes the delay of the logical circuit based on the delay time information in said delay analysis library".

Therefore, the system comprises only data (delay analysis library) and a software module (delay analyzing module). A system comprising software per se is not operational and functional without a computer. The specification as originally filed does not describe the system to include a computer apparatus. Therefore this claim cannot be patented under 35 USC 101. This amounts to functional descriptive material without having functional and structural relationship to otherwise statutory machine.

5.2 Claim 2 states, "A delay analysis system for making a delay analysis of a logic circuit, said system comprising:

a delay analysis library comprising connection information and delay time information for a plurality of circuits; and

a delay analyzing module which analyzes delays of the plurality of the circuits based on information in the delay analysis library, ….

wherein the delay analyzing module analyzes the delay of the logical circuit based on the delay time information in said delay analysis library".

Therefore, the system comprises only data (delay analysis library) and a software module (delay analyzing module). A system comprising software per se is not operational and functional without a computer. The specification as originally filed does not describe the system to include a computer apparatus. Therefore this claim cannot be patented under 35 USC 101. This amounts to functional descriptive material without having functional and structural relationship to otherwise statutory machine.

5.3 Claim 3 states, "A method of making delay analysis of a logical circuit, comprising:

referencing a delay analysis library for a plurality of circuits, said delay analysis library comprising connection information, delay time information and logic operation information, …; and

if the logic circuit comprises said at least one circuit, selecting a delay time of each path of said at least one circuit from said delay time information, …".

Therefore, the method comprises two steps of referencing a delay analysis library and selecting a delay time from delay time information in the library. A method listing mental steps is not patentable unless the method is implemented in a computer or an apparatus or transforms some material or article into a different state or thing. The application does not describe anywhere computer implementation of the method and does not show or describe a computer for implementing the method. Therefore this claim cannot be patented under 35 USC 101.

5.4 Claims 5 and 6 depend on the delay analysis system claim 1 and deal with the delay analysis module (a software module) but do not include any computer implementation of the software module. Therefore, they cannot be patented under 35 USC 101.

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hasegawa** (U.S. Patent 6,041,168) in view of **Hasegawa** (U.S. Patent 5,528,511).

8.1 **Hasegawa** '168 teaches high-speed delay verification apparatus and method therefor. Specifically, as per Claim 1, **Hasegawa** '168 teaches the delay analysis system for making a delay analysis of a logic circuit (CL1, L5-8); the system comprising:

a delay analysis library comprising connection information and delay time information for a plurality of circuits (CL1, L58-61 and CL2, L30-35); and

a delay analyzing module which analyzes delays of the plurality of the circuits based on information in the delay analysis library (Fig. 1, Item 7; CL4, L43-51; CL1, L58-61 and CL2, L30-35),

wherein, for at least one circuit of said plurality of circuits, said library further comprises logical operation information (CL1, L58-61 and CL2, L30-35),

wherein the delay analyzing module analyzes the delay of the logical circuit based on the delay time information in the delay analysis library (Fig. 1, Item 7; CL4, L43-51; CL1, L58-61 and CL2, L30-35).

**Hasegawa** '168 does not expressly teach that delay time information is provided for a signal path from input terminals to output terminals of a logical circuit and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at an output terminal, and wherein the delay time information for each signal path of the logical circuit of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to logical operation information. **Hasegawa** '511 teaches that delay time information is provided for a signal path from input terminals to output terminals of a logical circuit and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at an output terminal, and wherein the delay time information for each signal path of the logical circuit of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to logical operation information (Fig. 3; CL1, L28-35; CL2, L30-42; CL3, L5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output terminal; CL1, L28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; CL2, L30-42 states that the delay time of the upper route having

larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; CL3, L5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Hasegawa** '168 with the system of **Hasegawa** '511 that included delay time information provided for a signal path from input terminals to output terminals of a logical circuit and wherein delay time information was specific to an input terminal logical state transition and resulting logical state transition at an output terminal, and wherein the delay time information for each signal path of the logical circuit of the at least one circuit was based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to logical operation information, because this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process (CL2, L61-65).

8.2 As per Claim 2, **Hasegawa** '168 teaches the delay analysis system for making a delay analysis of a logic circuit (CL1, L5-8); the system comprising:

a delay analysis library comprising connection information and delay time information for a plurality of circuits (CL1, L58-61 and CL2, L30-35); and

a delay analyzing module which analyzes delays of the plurality of the circuits based on information in the delay analysis library (Fig. 1, Item 7; CL4, L43-51; CL1, L58-61 and CL2, L30-35),

wherein, for each of said plurality of circuits, said library further comprises logical operation information (CL1, L58-61 and CL2, L30-35),

wherein the delay analyzing module analyzes the delay of the logical circuit based on the delay time information in the delay analysis library (Fig. 1, Item 7; CL4, L43-51; CL1, L58-61 and CL2, L30-35).

**Hasegawa** '168 does not expressly teach that delay time information is provided for a signal path from input terminals to output terminals of a logical circuit and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at an output terminal for each circuit of said plurality of circuits, and wherein the delay time information for each signal path of the logical circuit of the plurality of circuits is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to logical operation information for the plurality of circuits. **Hasegawa** '511 teaches that delay time information is provided for a signal path from input terminals to output terminals of a logical circuit and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at an output terminal for each circuit of said plurality of circuits, and wherein the delay time information for each signal path of the logical circuit of the plurality of circuits is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals

corresponding to logical operation information for the plurality of circuits (Fig. 3; CL1, L28-35; CL2, L30-42; CL3, L5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output terminal; CL1, L28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; CL2, L30-42 states that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; CL3, L5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified).

8.3 As per Claim 3, **Hasegawa** '168 teaches a method of making delay analysis of a logical circuit (CL1, L5-8); comprising:

referencing a delay analysis library for a plurality of circuits, the delay analysis library comprising connection information, delay time information and logic operation information (CL1, L58-61 and CL2, L30-35).

**Hasegawa** '168 does not expressly teach that delay time information is provided for a signal path from input terminals of a logical circuit and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at each output terminal for at least one circuit of the plurality of circuits, the delay time information for each signal path of the at least one circuit is based upon logical state transitions at the input terminals

and corresponding logical state transitions at each output terminal as represented by logical operation information for the at least one circuit. **Hasegawa** '511 teaches that delay time information is provided for a signal path from input terminals of a logical circuit and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at each output terminal for at least one circuit of the plurality of circuits, the delay time information for each signal path of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at each output terminal as represented by logical operation information for the at least one circuit (Fig. 3; CL1, L28-35; CL2, L30-42; CL3, L5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output terminal; CL1, L28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; C2, L30-42 states that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; C3, L5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified).

**Hasegawa** '168 does not expressly teach if the logic circuit comprises the at least one circuit, selecting a delay time of each path of the at least one circuit from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the

delay time is selected based on the input terminal whose logical transition triggers the low state to high state transition of the selected output terminal according to the logical operation information or if a selected output terminal transitions from a high state to a low state the delay time is selected based on the input terminal whose logical transition triggers the high state to low state transition of the selected output terminal according to the logical operation information. **Hasegawa** '511 teaches if the logic circuit comprises the at least one circuit, selecting a delay time of each path of the at least one circuit from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on the input terminal whose logical transition triggers the low state to high state transition of the selected output terminal according to the logical operation information or if a selected output terminal transitions from a high state to a low state the delay time is selected based on the input terminal whose logical transition triggers the high state to low state transition of the selected output terminal according to the logical operation information (CL1, L28-35; CL2, L30-42; CL3, L5-26).

8.4 As per Claim 4, **Hasegawa** '168 teaches a computer-readable medium having stored thereon a program comprising computer instructions that, when executed on a computer, perform a process for executing a delay analysis method for a logic circuit, the computer-readable medium causing a computer to execute the method (CL1, L5-8); wherein the method comprises:

referencing a delay analysis library for a plurality of circuits, the delay analysis library comprising connection information, delay time information and logic operation information (CL1, L58-61 and CL2, L30-35).

**Hasegawa** '168 does not expressly teach that delay time information is provided for a signal path from input terminals of a logical circuit and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at each output terminal for at least one circuit of the plurality of circuits, the delay time information for each signal path of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at each output terminal as represented by logical operation information for the at least one circuit. **Hasegawa** '511 teaches that delay time information is provided for a signal path from input terminals of a logical circuit and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at each output terminal for at least one circuit of the plurality of circuits, the delay time information for each signal path of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at each output terminal as represented by logical operation information for the at least one circuit (Fig. 3; CL1, L28-35; CL2, L30-42; CL3, L5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output terminal; CL1, L28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; C2, L30-42 states that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; C3, L5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall

signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified).

**Hasegawa** '168 does not expressly teach if the logic circuit comprises the at least one circuit, selecting a delay time of each path of the at least one circuit from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on the input terminal whose logical transition triggers the low state to high state transition of the selected output terminal according to the logical operation information or if a selected output terminal transitions from a high state to a low state the delay time is selected based on the input terminal whose logical transition triggers the high state to low state transition of the selected output terminal according to the logical operation information. **Hasegawa** '511 teaches if the logic circuit comprises the at least one circuit, selecting a delay time of each path of the at least one circuit from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on the input terminal whose logical transition triggers the low state to high state transition of the selected output terminal according to the logical operation information or if a selected output terminal transitions from a high state to a low state the delay time is selected based on the input terminal whose logical transition triggers the high state to low state transition of the selected output terminal according to the logical operation information (CL1, L28-35; CL2, L30-42; CL3, L5-26).

**Hasegawa** '168 does not expressly teach performing a delay calculation to determine a propagation delay time using the selected delay time of the at least one circuit. **Hasegawa** '511

teaches performing a delay calculation to determine a propagation delay time using the selected delay time of the at least one circuit (CL3, L5-26).

### *Response to Amendments*

9. Applicants' arguments, filed on February 15, 2008 have been considered. Applicant's arguments with respect to claim rejections under 35 USC 103 (a) are not persuasive.

9.1 As per the applicants' argument that "Claims 1-4 recite, among other limitations, that the delay time information is specific to an input terminal logical state transition and resulting logical state transition at an output terminal of a logical circuit; the Examiner asserts that Hasegawa '511 teaches this required claim element; the Examiner is misinterpreting the teachings of Hasegawa '511; in the cited portions of Hasegawa '511 FIG. 3 shows a timing diagram for two inputs and an output of an OR gate; there is no delay time information in Hasegawa '511 which is specific to an input terminal logical state transition and a resulting logical state transition at an output terminal; the nullified states shown in Hasegawa '511, where no further action is required, are explicitly identified with respect to the state transitions at the input terminals and output terminal of the OR gate; the delay times shown in FIGS. 12 and 13 are identified between the input terminals 's' or 'v' and the output terminal 't'; with the configuration set forth in claim 1, a target point at which no further delay analysis is required is automatically determined; claim 1 was amended to recite that the delay analyzing module

analyzes the delay of the logical circuit based on the delay time information in said delay analysis library", the Examiner respectfully disagrees.

**Hasegawa** '511 shows at Fig. 3 the logical state transitions at each input terminal and logical state transitions at each output terminal. **Hasegawa** '511 discusses at CL1, L28-35 the logical state transitions at the input terminal and the output terminal, using rise/fall terms. **Hasegawa** '511 states at CL2, L30-42 that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid). The logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit. **Hasegawa** '511 describes at CL3, L5-26 that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified. Therefore, **Hasegawa** '511 teaches a delay time information that is specific to an input terminal logical state transition and resulting logical state transition at an output terminal, as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (CL2, L61-65).

***Conclusion***

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is

571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez, can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Kandasamy Thangavelu/
Art Unit 2123
July 1, 2008